Methods and Misconceptions in Teaching VHDL

Mizrahi S.
Jerusalem College of technology, Electronics wing, York University

Abstract

The teaching of Hardware Description Language as VHDL or VERILOG became a part of the curriculum of the electronics engineering and technical engineering studies. All so there is trend to teach these languages in technical hi schools.

Many lecturers talk and write about the difficult and misconceptions in the understanding of HDL's, but only few of them saged ways to improve the quality of learning and understanding. This article describes a research on the reasons for HDL misconceptions and the ways to avoid them.

1. Introduction

1.1 What is VHDL and what is deference to other programming languages?

VHDL and VERILOG are Hardware Description Languages; they used to describe the structure and the functionality of electronic circuits and systems. The syntax of VHDL and VERILOG is very similar to programming languages as C or PASCAL. The programming languages made for describing sequential process, this is one of the main efforts of computer teachers in teaching beginners that the CPU executing line after line and there is mining to the lines order. In counter HDL don't have mining to line order, and if you want to make a sequential process you have to use special directive for it.

For example:

VHDL          C
1) A<=B;        1) A=B;
2) C<=D;        2) C=D;

In programming language, line 1 is executed before line 2. In VHDL the tow lines are executed in the same time. If I want to be accurate in HDL there is no execution, every line is hardware that work on parallel.
HDL looks like programming language, but it is a hardware description language. Here are some more examples of VHDL and similar C code, and we can see the big different in the mining of the code:

When we write a C function this function will change the value of O only on the function call.

```c
C_Function()
{
  if (S==1) O=A;
      else O=B;
}
```

But when we write a VHDL code with similar syntax the result will be totally different, we crate hardware!

```vhdl
process (S)
begin
  if (S='1') then O<=A;
      else O<=B;
  end if;
end process;
```

We can see that with the hardware was created by the VHDL code; O will change value all the time

Second example

```c
C_Function2(char A)
{
  for ( I=0 ;I<3;I++)
  {
    if (A == I)
        O(I) = 1;
    else   O(I) = 0;
  }
}
```

In this C function only on the function call the O Bits will rise to 1.

The VHDL syntax is very similar but the mining is totally different.
process (A)
begin
  for I in 0 to 3 loop
    if (A = I) then
      O(I) <= '1';
    else
      O(I) <= '0';
    end if;
  end loop;
end process;

The hardware created from this code is a multiple output with different conditions, each output has its condition and it operates in parallel with all other outputs. Here we can start to understand the reasons for this research.

Student after years of learning sequential programming, and efforts made to teach them think sequentially, they start to learn a language that only looks like a programming language, then the student is trying to use his old knowledge (knowledge transfer) and it doesn't work (sometimes!).

1.2 Research objective

The research objective was to construct an effective model of teaching VHDL, a model that utilizes the previous courses in the Department of Electronic Engineering. To achieve the research objective it was necessary to achieve a number of intermediate goals:

A. To discover the points of difficulty of the learning of the VHDL language.
B. To focus on what are the pre-conditions of the learning of the VHDL language.
C. To identify the primary emphases that should be addressed when teaching the VHDL language.
D. To search for ways and to build models for teaching the language according to the target populations of the students.
When we come to make a research on misconceptions and the ways to avoid them, we need to examine the learning environment and the learning process. The mining of learning environment is mainly the lecturer and the tools he use. The mining of learning process is the Way the student gets the learning environment. In the framework of the present research, we examined the research questions from three directions.

A. The collection and analysis of information in regards to teaching methods and approaches in universities around the world, at the Technion in Israel, at JCT in Israel, and in practical engineering schools in Israel.

B. Review of a considerable number of the textbooks accepted in the teaching of VHDL. We performed analysis of the material presented in the books from different aspects such as the order of instruction, contents, and teaching approaches and whether it is based on hardware view or whether the HDL language is taught as a programming language.

C. The analysis of the achievements of students in the VHDL course in JCT. (30 students)

D. The analysis of achievements and difficulties of the performers of the final projects in the VHDL field in JCT. (10 projects)

Another direction examined in the framework of this research was performed

2. Research and Conclusions

2.1 The Points of Difficulty in the Study of the VHDL Language

In the research, several sources of information allowed us to focus on the difficulty of learning the VHDL language.

The first source was the articles and learning materials of VHDL course from several universities over the world. Most of them begin with the presentation of the difficulty of learning of this language. Here are some of the phrases used to describe the difficulties in learning of VHDL:
Those people who have learned C to forget everything (Dr. Adnan Shaout of the University of Michigan – Dearborn). Think in parallel about the possible implementation in hardware (A Short Description of the VHDL Language(Hebrew), Technion IL). Refresh the knowledge in Digital Systems and Design before engage in the study of the VHDL language (Zwolinski, 2000). In the preface to his book, Havarvar (2005) cites the difficulty that the learners face in the coping with the VHDL language but does not focus it on a certain difficulty point. It can be summarized that many of the instructional books present the problems entailed by the learning of VHDL but do not present the focus of the problem and the difficulty in the learning of the language.

The second was the processing of the results of a test held for the graduate of the course in VHDL, 30 students. From the analyses of the test results and the correlation between the different abilities tested. The question that tested the ability of hardware view had the lowest mean and the highest standard deviation. This indicates significantly that the students have difficulty with the hardware view and in the case of the test, primarily the students from the weaker group.

The third was the analysis of interviews conducted with students performing final projects, 10 projects. From the summary of the interviews with the students and follow up after the project performance, it can be determined that the students have a fundamental problem of hardware view, unlike the researcher’s first assumption that the problem in the understanding of the language derives from the understanding of the concepts of synchronous and asynchronous systems. In addition, the problem is more prominent among the students with low achievements, when the lack of linkage between the written code and the understanding of the hardware sometimes induces confusion of the concepts and absolute approach to the VHDL code as software.

The follow up after the students shows that there is difficulty differentiating between synchronous writing and asynchronous writing. In addition, there is difficulty writing state machines, but it appears that it derives from a more entrenched problem of internalization that VHDL is a hardware description language that looks like a programming language.

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1. www-personal.engin.umd.umich.edu/~shaout/Introduction-to-VHDL.ppt
2.2 What Are the Pre-Conditions for the Learning of the VHDL Language?

We presented in the review of the literature and the research a number of attempts to teach VHDL as a programming language. However, it appears that the people who go in this direction encounter many difficulties, as noted by Shaout in his introduction to the course. In addition, our research among students shows that the primary difficulty is the development of the hardware view ability. Hence, the Digital Systems Design course is an essential and necessary pre-condition of the course in VHDL. In addition, it is important that in the prerequisite course the students learn well the state machines which are part of the study material in the VHDL course.

It should be noted that programming courses are a disruptive factor in the understanding and perception of the VHDL language, which by nature is a parallel language, since the hardware works in parallel, in contrast to other programming languages, which are generally sequential. In addition, the code in VHDL creates hardware or relationships in the hardware that perform the process. In contrast, in programming languages the hardware does not experience any change in the programming process. These differences in the understanding make it difficult for the students to achieve high-level developments in VHDL and this fact must be taken into account. Therefore, the emphases that appear in the following passage are essential to the teaching of a hardware description language.

2.3 Primary Emphases in the Teaching of the VHDL Language

Our research shows that there indeed is a problem of the erroneous perception of what is learned in the VHDL lessons. This mistaken perception is evinced primarily in situations in which the student is required to realize systems that they have not encountered in the course framework and the system needs to combine sequential and parallel processes. Our research shows that the problem in the erroneous perception derives from the approach to VHDL as software and not as a hardware description language. Therefore, in the teaching of the language we need to perform actions that will turn the learner’s attention to the fact that he is addressing hardware.
The results of the research of the interviews with the students who are performing a project show that running a test bench and presenting a waveform were not sufficient to clarify what happens inside the component. The lower the student’s level was, the more important it was to use a schematic view and block diagrams.

Our research shows that to achieve understanding it is very necessary and important to present to the students the results of the synthesis and how it is related to the code written. It is recommended not to illustrate this according to large passages of code so that the schema created will be readable and understandable. In addition, it is possible to perform the synthesis and place and route for the target components, which are CPLD and not FPGA, in which the results of the synthesis will be clearer and more understood.

The study of the topic only through computer and simulations increases the chance for erroneous perception and therefore it is essential that the exercises on true hardware, including downloading the code to a real component, be performed a number of times during the course to strengthen the hardware view of the study material.

Our research is reinforced by additional works, such as the research of Hussein, Gruenbacher, and Noureddin (1999). But they had less than ten students on their research.

Beyond the aforementioned statements, the recommendations made by Ben Ari (2000) for the planning of the teaching in computer science are also valid for VHDL. However, the target components are not CPU processors but CPLD or FPGA. Here are Ben Ari recommendations changed by the researcher to fit VHDL.

1. It is necessary to teach a model of the target hardware that explicitly addresses the structure of the hardware and the flow of signals. The question is what the required level of detail is and what component to use CPLD or FPGA there are several perceptions on this issue. This type of model will support the understanding of how a VHDL code is place & routed on a component.

2. An essential model of the CPLD / FPGA should be taught before the abstraction.
3. It is prohibited that the tempting reality of the components CPLD / FPGA will take the place of the construction of the model.

4. The fact that there are different approaches for design and programming must be acknowledged, from top down programming to bottom up and bricolage. However, the use of bricolage without an appropriate model and a good understanding of the concepts and practice can disrupt beginning students.

5. Laboratory assignments allow the student to be active and to construct knowledge on the basis of his experience. Therefore, it is preferable to combine closed assignments and the type of assignment should encourage cognitive processes such as analysis, examination of possibilities, and decision making.

6. Attention should be given to the method of evaluation. In contrast to the tests in which the results are evaluated, evaluation in computer science should address not only the product but also, primarily, the process of problem solving.

3. Summary

In the framework of this research, we studied the primary factors of the erroneous perception among students who learn the VHDL language. The development of a hardware view will significantly reduce the deficiencies evinced in the study of the VHDL language. In this research, we present additional sources that reinforce the research results.

In the discussion of the research results, we present a number of practical conclusions on how to recommend learning the VHDL language. The primary recommendations revolve on the focus of the students on their understanding that in their writing they create hardware. This focus is supposed to be expressed in correct use of the development tools and the download to the real component of the exercises performed by the students, at least a number of times during the course.
Bibliography


**Web sites on project oriented learning**

6. [http://www.samford.edu/pbl/definitions.html](http://www.samford.edu/pbl/definitions.html)

7. [http://www.cet.edu/earthinfo/classroom/teachers/FTtopic1.html](http://www.cet.edu/earthinfo/classroom/teachers/FTtopic1.html)